

Figure 1

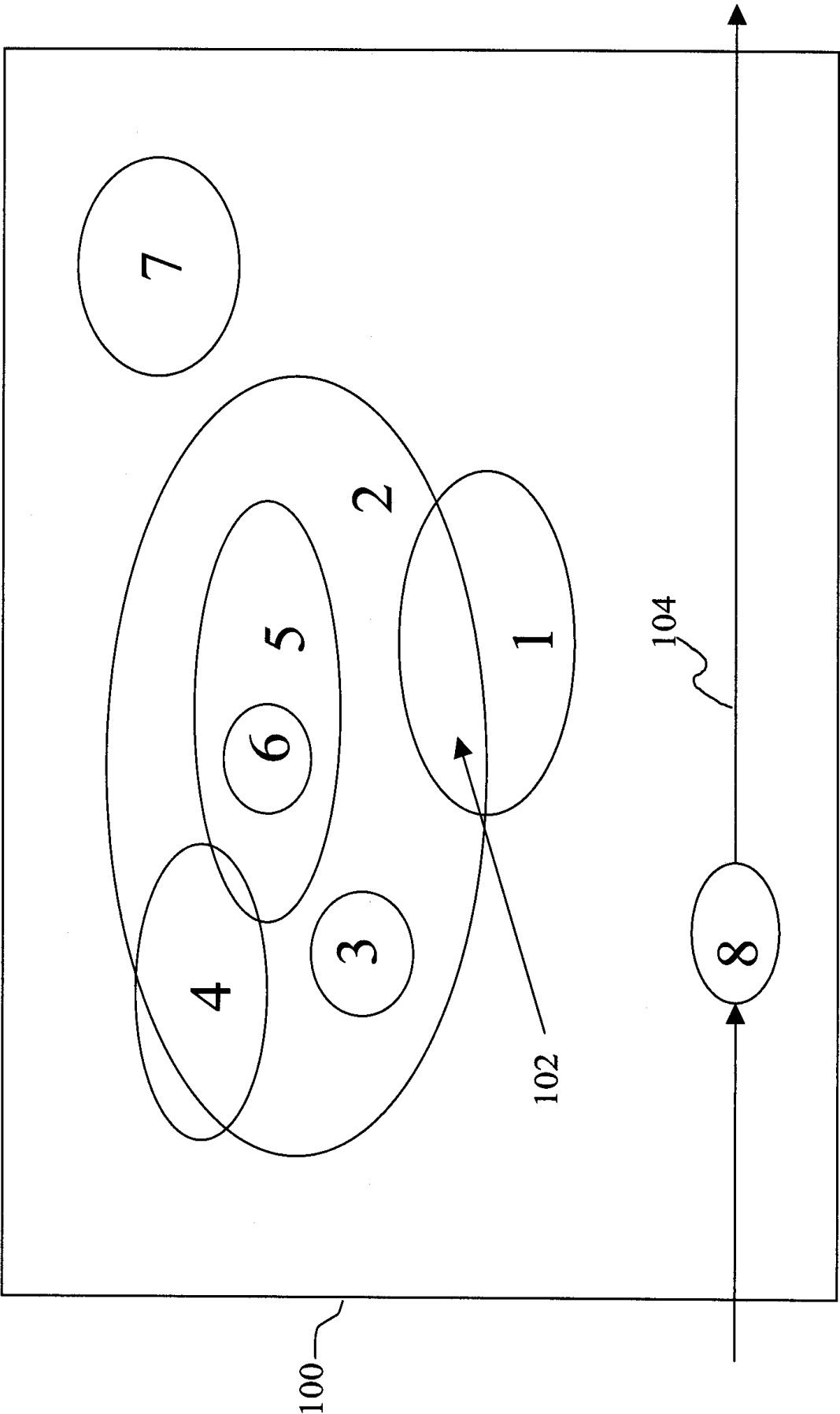


Figure 2

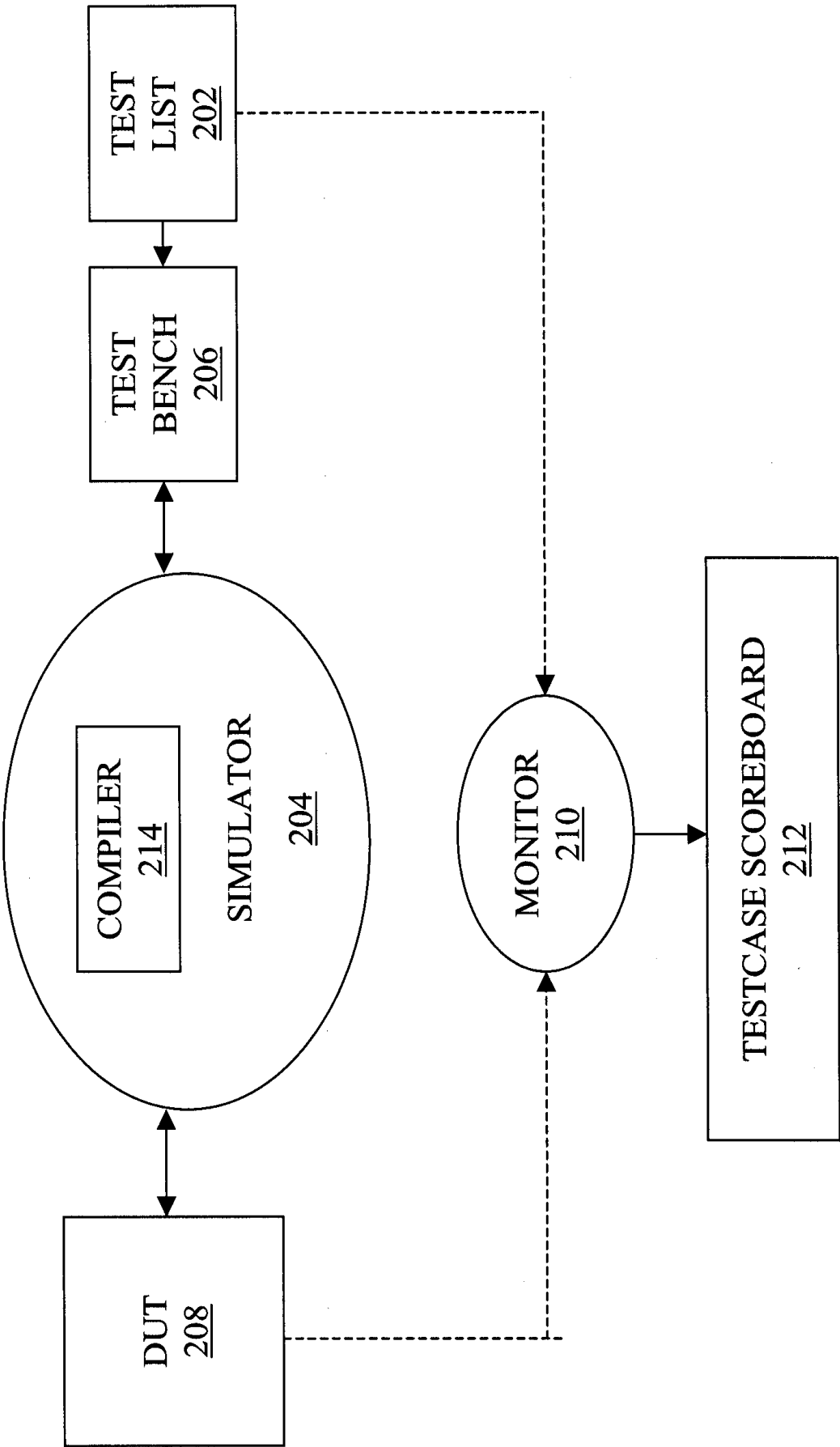


Figure 3a

LOGIC	LOGIC	LOGIC	LOGIC	LOGIC	LOGIC	LOGIC
AREA	AREA	AREA	AREA	AREA	AREA	AREA
1	2	3	4	5	6	

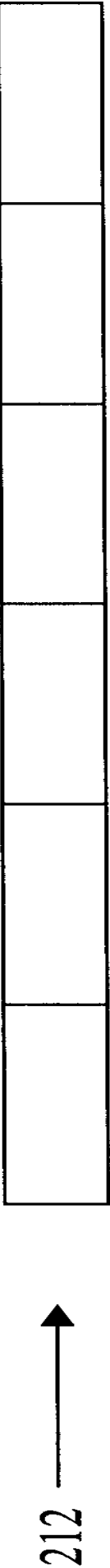


Figure 3b

	LOGIC AREA 1	LOGIC AREA 2	LOGIC AREA 3	LOGIC AREA 4	LOGIC AREA 5	LOGIC AREA 6
Testcase A	X		X		X	
Testcase B			X	X		
Testcase C			X	X		X
Testcase D	X	X				
Testcase E		X			X	
Testcase F			X			
⋮						
Testcase X						X



# Figure 4

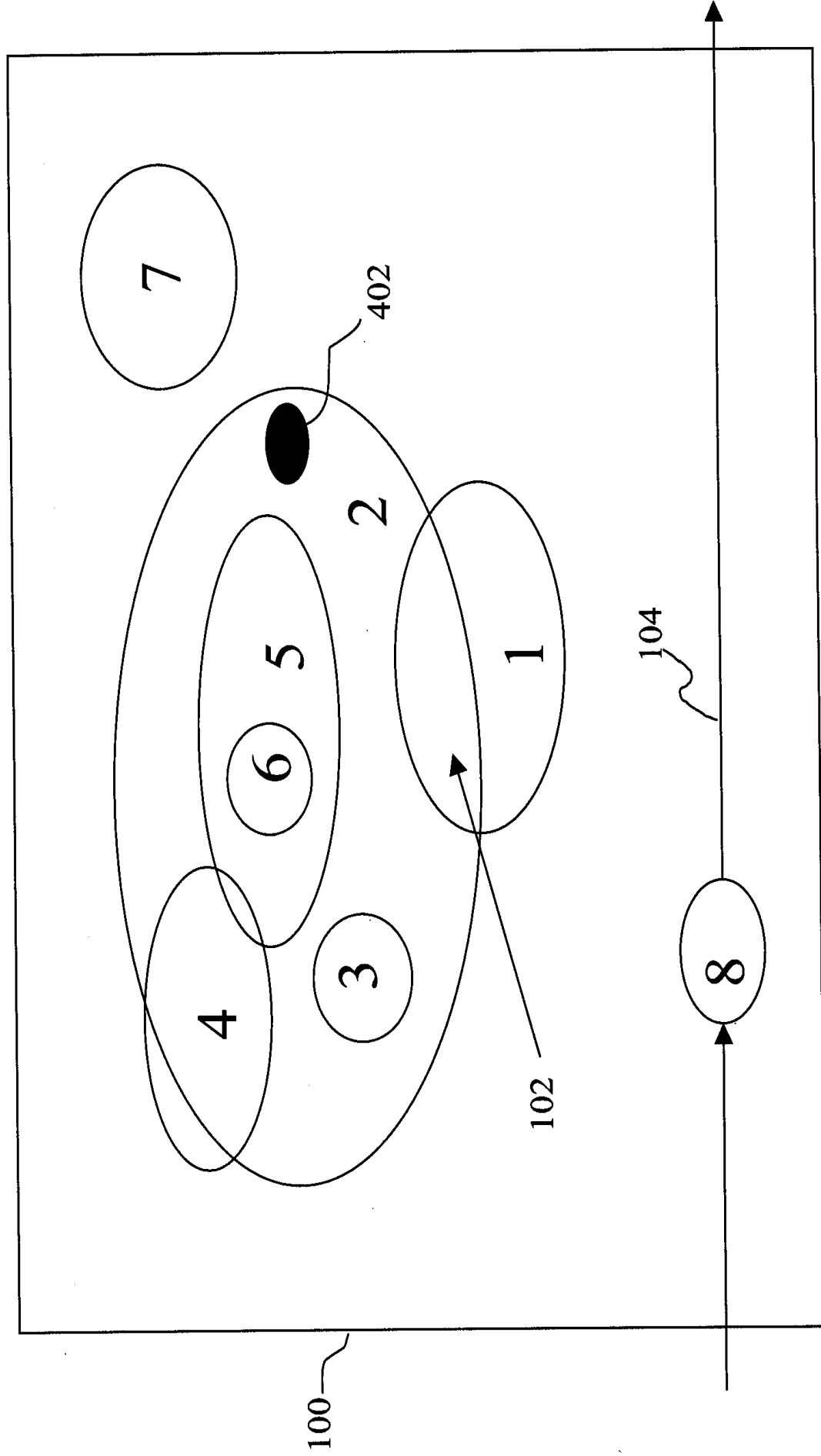


Figure 5a

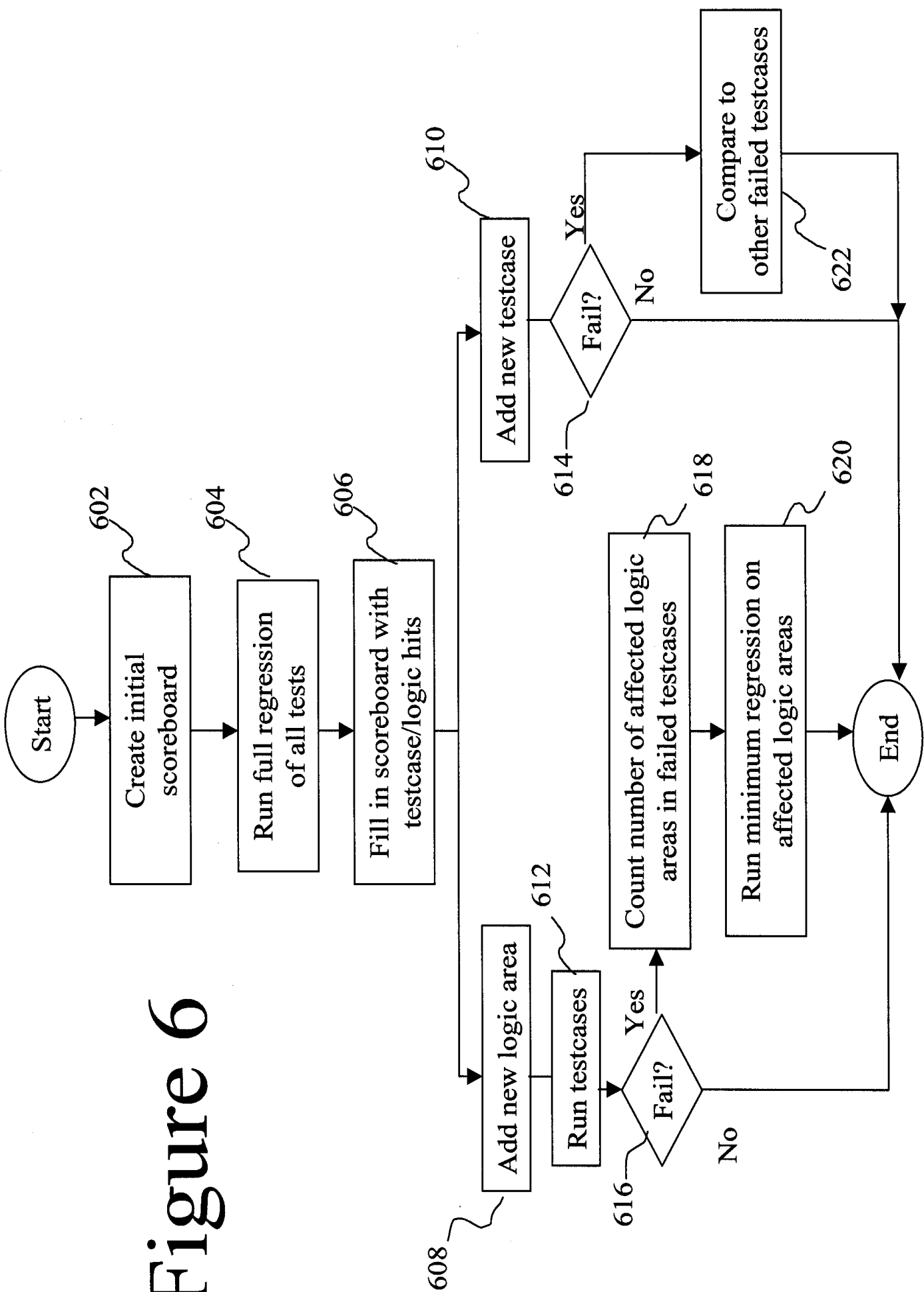
	LOGIC AREA 1	LOGIC AREA 2	LOGIC AREA 3	LOGIC AREA 4	LOGIC AREA 5	LOGIC AREA 6
PASS Testcase A	X		X		X	
PASS Testcase B			X	X		
PASS Testcase C			X	X		X
FAIL Testcase D	X	X				
FAIL Testcase E		X			X	
PASS Testcase F			X			
⋮						
PASS Testcase X						X

TOTAL	1	2	0	0	1	0
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Figure 5b

	LOGIC AREA	LOGIC AREA	LOGIC AREA	LOGIC AREA	LOGIC AREA	LOGIC AREA
	1	2	3	4	5	6
FAIL Testcase A	X		X	X	X	
PASS Testcase B			X	X		
PASS Testcase C			X	X		X
FAIL Testcase D	X	X				
FAIL Testcase E		X			X	
PASS Testcase F			X			
⋮						
PASS Testcase X						X

Figure 6





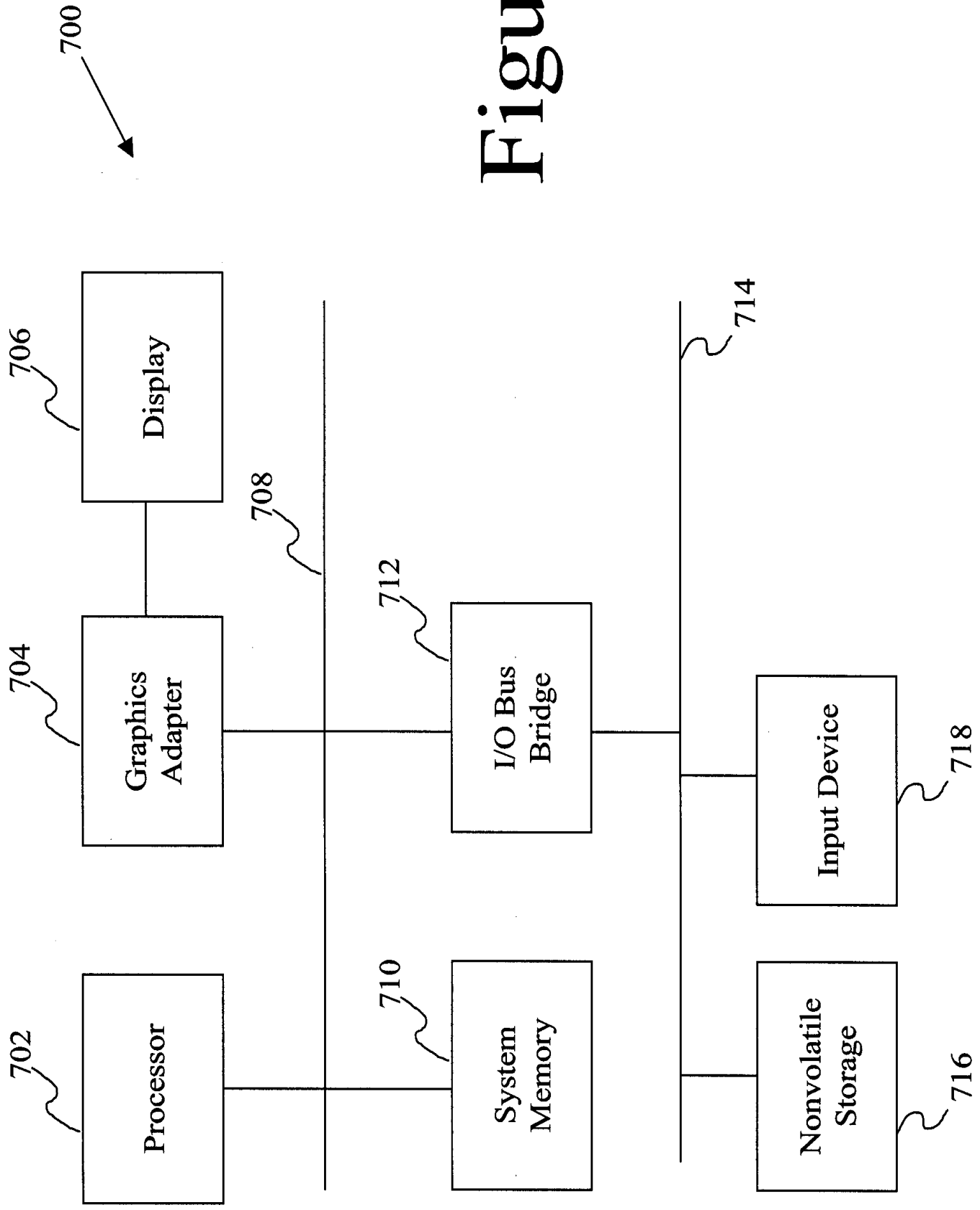


Figure 7